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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,715	03/15/2004	Toyokazu Fujii	60188-756	8984

7590 07/07/2005

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EXAMINER	
PHAM, THANHHA S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 07/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,715	FUJII ET AL.	
	Examiner	Art Unit	
	Thanhha Pham	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *34-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *34-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/018,181.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to Applicant's Amendment dated 06/20/2005.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. **Claims 34-48 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.** The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Limitation of "a silicon oxide film in contact with a second region of said upper surface of said insulating film, said silicon oxide film not including said impurity/said phosphorus" is not supported by specification and figures.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 34-46 are rejected under 35 U.S.C. 102(b) as being anticipated by Itoh et al [US 5,160,998].

► With respect to claims 34 and 36-37, Itoh et al. (fig. 5e, abstract, col. 1-9) discloses the claimed semiconductor device comprising:

a substrate (1) having a semiconductor region ***[claim 34]***;

an insulating film (412, BPSG, col. 4 line 36) formed on said semiconductor region, said insulating film including impurities comprising boron and phosphorous ***[claims 34, 36 and 37];***

an interconnection (32) disposed on and in contact with a first region of an upper surface of said insulating film (412);

a silicon oxide film (421, SiO_2, col 5 lines 11-18 and col. 4 line 18) in contact with a second region of said upper surface of said insulating film (412), said silicon oxide film not including said impurities;

a silicon nitride film (422, Si_3N_4, col. 5 lines 11-18 and col. 4 line 36) formed on said silicon oxide film (421).

► With respect to claim 35, the insulating film (412, BPSG) of Itoh et al has a property of reflowing due to a heat treatment under predetermined conditions.

► With respect to claims 38-39, Itoh et al. (fig. 5e) shows that the surface of the insulating film (412) is planarized.

► With respect to claims 40-41, Itoh et al. (fig. 5e) shows that wherein substantially the entire lower surface of said silicon nitride film (422, Si_3N_4) is in contact with an upper surface of said silicon oxide film (421, SiO_2).

► With respect to claim 42, Itoh et al. (fig. 5e) discloses that a part of the silicon oxide film (421, SiO_2) formed over the interconnection (32); and a part of silicon nitride film (422, Si_3N_4) formed on said silicon oxide film (421, SiO_2).

► With respect to claim 43, Itoh et al. (fig. 5e, abstract, col. 1-9) discloses the claimed semiconductor device comprising:

a substrate (1) having a semiconductor region;

an insulating film (412, BPSG, col. 4 line 36) formed on said semiconductor region, said insulating film including phosphorous;

an interconnection (32) disposed on and in contact with a first region of an upper surface of said insulating film (412);

a silicon oxide film (421, SiO_2, col 5 lines 11-18 and col. 4 line 18) in contact with a second region of said upper surface of said insulating film (412);

a silicon nitride film (422, Si_3N_4, col. 5 lines 11-18 and col. 4 line 36) formed on said silicon oxide film (421).

► With respect to claim 44, Itoh et al. (fig. 5e) discloses that an upper insulating film (432, col. 5 lines 19-24 and col. 4 lines 36) including impurities is formed on the silicon nitride film (422, Si_3N_4).

► With respect to claim 45, Itoh et al. (fig.5e) shows a surface of the upper insulating film (432) is planarized.

► With respect to claim 46, Itoh et al (fig. 5e, cols 1-4) discloses the silicon oxide film as the tensile stress insulating layer (421, SiO_2, col 5 lines 11-18 and col. 4 line 18) underneath a silicon nitride as compressive stress insulating film (422, Si_3N_4, col. 5 lines 11-18 and col. 4 line 36). The silicon oxide film (421) of Itoh et al. provides tensile stress for the silicon nitride (422).

3. Claims 34-36 and 38-45, as being best understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Mayumi et al. [JP 61287151]

► With respect to claim 34, Mayumi et al. (fig. 1, abstract, text pages 1-2) discloses the claimed semiconductor device comprising:

a substrate (1) having a semiconductor region;

an insulating film (2) formed on said semiconductor region, said insulating film including impurities;

an interconnection (3) disposed on and in contact with a first region of an upper surface of said insulating film (2);

a silicon oxide film (4) in contact with a second region of said upper surface of said insulating film (2);

a silicon nitride film (5) formed on said silicon oxide film (4).

► With respect to claims 35-36, Mayumi et al. (fig. 1, abstract) discloses that the insulating film (2) includes phosphorus. The insulating film (2, PSG) would have property of reflowing due to a heat treatment under predetermined conditions.

► With respect to claims 38-39, Mayumi et al. (fig. 1) shows that the surface of the insulating film (2) is planarized.

► With respect to claims 40-41, Mayumi et al. (fig. 1) shows that wherein substantially the entire lower surface of said silicon nitride film (5) is in contact with an upper surface of said silicon oxide film (4).

► With respect to claim 42, Mayumi et al. (fig. 1) discloses that a part of the silicon oxide film (4) formed over the interconnection (3); and a part of silicon nitride film (5) formed on said silicon oxide film (4).

► With respect to claim 43, Mayumi et al. (fig. 1, abstract, text pages 1-2) discloses the claimed semiconductor device comprising:

a substrate (1) having a semiconductor region;

an insulating film (2) formed on said semiconductor region, said insulating film including phosphorous;

an interconnection (3) disposed on and in contact with a first region of an upper surface of said insulating film (2);

a silicon oxide film (4) in contact with a second region of said upper surface of said insulating film (2);

a silicon nitride film (5) formed on said silicon oxide film (4).

► With respect to claim 44, Mayumi et al. (fig. 1) discloses that an upper insulating film (6) including impurities is formed on the silicon nitride film (5).

► With respect to claim 45, Mayumi et al. (fig.1) shows a surface of the upper insulating film (6) is planarized.

4. Claims 34-43 and 48, as being best understood, are rejected under 35 U.S.C. 102(e) as being anticipated by Ueda et al. [US 5,545,919].

► With respect to claim 34, Ueda et al. (fig. 11, cols 1-11) discloses the claimed semiconductor device comprising:

a substrate (10, col. 1 lines 40-45) having a semiconductor region;

an insulating film (14, col. 1 lines 47-51) formed on said semiconductor region, said insulating film including impurities;

an interconnection (3,col. 1 lines 53-56) disposed on and in contact with a first region of an upper surface of said insulating film (14);

a silicon oxide film (1, col. 1 lines 59-62) in contact with a second region of said upper surface of said insulating film (14);

a silicon nitride film (2, col. 1 lines 59-62) formed on said silicon oxide film (1).

► With respect to claims 35-37, Ueda et al. (col. 1 lines 47-51) discloses that the insulating film (14) includes phosphorus and boron. The insulating film (14, BPSG) would have property of reflowing due to a heat treatment under predetermined conditions.

► With respect to claims 38-39, Ueda et al. (fig. 11, col. 1 lines 47-51) shows that the surface of the insulating film (14) is planarized.

► With respect to claims 40-41, Ueda et al. (fig. 1) shows that wherein substantially the entire lower surface of said silicon nitride film (2) is in contact with an upper surface of said silicon oxide film (1).

► With respect to claim 42, Ueda et al. (fig. 1) discloses that a part of the silicon oxide film (1) formed over the interconnection (3); and a part of silicon nitride film (2) formed on said silicon oxide film (1).

► With respect to claim 43, Ueda et al. (fig. 11, cols 1-11) discloses the claimed semiconductor device comprising:

a substrate (10, col. 1 lines 40-45) having a semiconductor region;

an insulating film (14, col. 1 lines 47-51) formed on said semiconductor region, said insulating film including phosphorous;

an interconnection (3,col. 1 lines 53-56) disposed on and in contact with a first region of an upper surface of said insulating film (14);

a silicon oxide film (1, col. 1 lines 59-62) in contact with a second region of said upper surface of said insulating film (14);

a silicon nitride film (2, col. 1 lines 59-62) formed on said silicon oxide film (1).

► With respect to claim 48, Ueda et al. (fig. 11) shows a gate electrode (12) is formed over said semiconductor region and said insulating film (14) is formed over said gate electrode (12).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 47, as being best understood, is rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda et al. [US 5,545,919] in view of Douglas [U.S. Pat. 4,807,016].

Ueda et al. substantially discloses all the limitations as claimed above except teaching that the insulating film (14) includes phosphorus which concentration is 3.0 wt% or more. However, Douglas discloses that the insulating film (BPSG) typically includes approximately 1 to 10 by weight of phosphorus in their chemical formula (see col. 1, lines 39-43). The concentration range would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990). Therefore, at the time of invention, it would have been obvious to the skilled in the art, in view of Douglas, to use the insulating film including concentration of 3.0% or more in the semiconductor device of Ueda et al. to provide isolation function as desired in the semiconductor device.

6. Claim 46, as being best understood, is rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda et al. [US 5,545,919] or Mayumi et al. [JP 61287151] as applied to claim 43 above in view Itoh et al. [US 5,160,998].

Ueda et al. and Mayumi et al. substantially discloses the claimed semiconductor device but fails to recognize the characteristics of the silicon oxide film (PSG) for

providing tensile stress for the nitride film. Ueda et al and Mayumi et al generally recognize that the silicon oxide film (PSG) is used to prevent disconnection of the interconnection and prevent crack generation.

However, Itoh et al. (fig. 5e, cols 1-4) recognizes using the silicon oxide film (either with or without impurities/phosphorous) as the tensile stress insulating layer (411) underneath a silicon nitride as compressive stress insulating film (412) would prevent crack generation in the insulation layers and disconnection in the interconnection. The silicon oxide film (411) of Itoh et al. provides tensile stress for the silicon nitride (412).

Therefore, at the time of invention, it would have been obvious for those skilled in the art, in view of Itoh et al, to have the silicon oxide film in the semiconductor device of Ueda et al or Mayumi et al with characteristics of providing tensile stress for the silicon nitride as being claimed to prevent crack generation and interconnection disconnection in the semiconductor device (see Itoh et al.: col. 2 lines 20-35 and col. 4 lines 13-41 for details).

7. Claims 47-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itoh [US 5,160,998] in view of Ueda et al [US 5,545,919].

► With respect to claim 48, the claimed range phosphorous concentration of the insulating film is considered However, the claimed range distance for the via penetrating the metal line is considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in In re Aller 105 USPQ233, 255

(CCPA 1955), the selection of reaction parameters such as temperature and concentration would have been obvious.

> "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed "critical ranges and the applicant has the burden of proving such criticality... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."
>
> *See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).*

► With respect to claim 48, Itoh et al substantially discloses the claimed semiconductor device but does not expressly discloses a gate electrode is formed over said semiconductor region and said insulating film is formed over said gate electrode.

However, Ueda et al. (fig. 11) shows a gate electrode (12) is formed over said semiconductor region and said insulating film (14) is formed over said gate electrode (12).

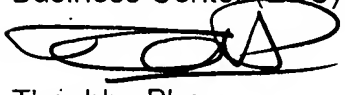
Therefore, at the time of invention, it would have been obvious for those skilled in the art to modify the semiconductor of Itoh et al to include the gate electrode as being claimed, per taught by Ueda et al, to provide appropriate operation in the semiconductor device as being needed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham whose telephone number is (571) 272-1696. The examiner can normally be reached on Monday and Thursday 9:00AM - 9:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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